Francisco Braga

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Education

Masters of Applied Science, Electrical Engineering — Sep 2024 - May 2026
Toronto Metropolitan University — *GPA: 4.08/4.33*

Bachelor of Engineering, Electrical Engineering — Sep 2020 - May 2024
Toronto Metropolitan University — *GPA: 3.73/4.33*

Experience

Graduate Researcher — Sep 2024 – Present
Toronto Metropolitan University

- Advanced graduate research in low voltage conversion ultra-low power ADCs.
- Developed various energy efficient mixed-mode ADC blocks operating in subthreshold using ultra-low supply voltage, and power gating for sub 3mV input voltage conversions.
- Enhanced existing oscillator, arbiter, amplifiers and timing circuits in multiple relevant performance metrics.
- Achieved an ADC conversion efficiency improvement of 51% compared to existing architectures.

Teaching Assistant — Sep 2024 – Present
Toronto Metropolitan University

- Directed tutorial sessions on various circuit topics across 1st to 3rd year circuits courses, for over 200 students.
- Conducted numerous lab sessions focused on teaching key circuit concepts using lab equipment to students.

Research Assistant — May 2023 – Aug 2023
Smart Microgrid Resiliency, Toronto Metropolitan University

- Participated in microgrid simulation model creation using Typhoon HIL and tested models using SCADA panels.
- Designed protection schemes to combat malicious grid effects such as overcurrent, and undervoltage.
- Applied coordination into protection system to ensure sub 20ms response for preservation of DER stability.

Projects

Ultra-Low Power Hybrid ADC with PT Compensation | *Cadence Virtuoso* — Sep 2025

- Designed and simulated a 5-bit Hybrid ADC consisting of a VTC, Vernier TDC, and process-temperature sensor, operating at 100kS/s with differential inputs of 1.56mV, on TSMC 130nm 1.2V CMOS technology.
- Developed analog layouts for oscillators, amplifiers, voltage bias blocks, and clocking circuits in 130nm CMOS.
- Optimized ADC performance by using post-layout extraction and reducing critical parasitic impacts.
- Achieved ENOB of 4.5, power consumption of 2.28μW, FOM of 1.01 fJ/conv., and SINAD of 22.86 dB.

Capstone: Low-Power Hybrid ADC | *Cadence Virtuoso* — May 2024

- Designed and simulated a 12-bit SAR ADC consisting of a 8-bit SAR ADC and a 4-bit Vernier TDC, operating at 100kS/s with VFSR 400mV, on TSMC 130nm 1.2V CMOS technology.
- Achieved ENOB of 11.54, along with a SINAD of 71.27dB and power consumption of 1.28mW.
- Designed clocking for system by creating a DLL to operae with a reference clock of 100kHz, created phase detector, up/dn counter, and delay line blocks to meet timing requirements and limit power consumption.

CMOS Capacitively-Coupled Instrumentation Amplifier | *Cadence Virtuoso* — Nov 2023

- Designed a high-swing telescopic cascode op amp in accordance with constraints and design specifications.
- Performed compehensive performance evaluation on design to evaluate overall performance via output swing, slew rate, output impedance, AC gain and phase, transient analysis, signal spectrum, and noise spectral density.
- Achieved compliance and exceeded 90% of specifications through identification of key design trade-offs.

MOSFET Gate Driver PCB | *Altium Designer* — Aug 2022

- Designed MOSFET Isolator Gate Driver board for rover motor control and main PCB integration.
- Used Altium to create footprints for all components, designing the PCB, schematics, and selecting components.
- Coordinated with senior team lead to arrange meetings, as well as progress discussions and updates.

Technical Skills

Tools: Cadence Virtuoso, Altium Designer, EAGLE, EasyEDA, Microcontrollers, Lab Equipment
Programming: Python, C, Assembly x86, MATLAB, SIMULINK, VHDL